IN THE CLAIMS

Please amend claims 14 and 16 as follows below.

Please add new claims 33-37 as follows below.

MARKED UP CLAIMS LISTING

1-13. (Cancelled)

14. (Currently Amended) An instruction set architecture (ISA) for execution of operations within a digital signal processor to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples, the instruction set architecture comprising:

a set of instructions for operation within a digital signal processor wherein each instruction includes a first operand accessed directly from memory, a second operand accessed directly from memory of a local register, and a destination register to store results, the set of instructions including,

a 20-bit DSP instruction, and

a 40-bit DSP instruction,

the set of instructions to accelerate calculations within the digital signal processor of the type where D = [(A operation one B) operation

two C) where operation one and operation two are separate signal processing operations.

15. (Previously Presented) The instruction set architecture (ISA) of claim 14 for execution of operations within a digital signal processor, wherein,

the twenty bit instruction uses mode bits in control registers and the forty bit instruction has a control extension to override the mode bits.

16. (Currently Amended) An instruction set architecture (ISA) for execution of operations within a digital signal processor <u>to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples</u>, the instruction set architecture comprising:

a set of instructions for operation within a digital signal processor wherein each instruction includes a first operand accessed directly from memory, a second operand accessed directly from memory of a local register, and a destination register to store results, the set of instructions including,

a 20-bit DSP instruction,

a 40-bit DSP instruction, and

a dyadic instruction to execute two operations in one instruction;

the set of instructions to accelerate calculations within the digital signal processor of the type where D = [(A operation one B) operation two C] where operation one and operation two are separate signal processing operations.

17. (Original) The instruction set architecture (ISA) of claim 16 for execution of operations within a digital signal processor, wherein

the two operations of the dyadic instruction for execution in one instruction are DSP operations.

18. (Original) The instruction set architecture (ISA) of claim 17 for execution of operations within a digital signal processor, wherein

the DSP operations are of the set of operations of multiplication, addition, extremum, and no operation.

19-20. (Cancelled)

21. (Previously Presented) The instruction set architecture (ISA) of claim 15 for execution of operations within a digital signal processor, wherein,

the control registers are mode registers.

22-29. (Cancelled)

30. (Previously Presented) The instruction set architecture (ISA) of claim 14 for execution of operations within a digital signal processor, wherein

the digital signal processing operations are of the set of operations of multiplication, addition, extremum, and no operation.

31. (Previously Presented) The instruction set architecture (ISA) of claim 16 for execution of operations within a digital signal processor, wherein,

the twenty bit instruction uses mode bits in control registers and the forty bit instruction has a control extension to override the mode bits.

32. (Previously Presented) The instruction set architecture (ISA) of claim 31 for execution of operations within a digital signal processor, wherein,

the control registers are mode registers.

33. (New) An instruction set architecture (ISA) for voice over internet protocol (VOIP), the instruction set architecture comprising:

a set of instructions for operation within a digital signal processor to convert between samples and packets for voice and data communication over a network, wherein each instruction includes a first operand accessed directly from memory, a second operand accessed directly from memory of a local register, and a destination register to store results, the set of instructions including,

a 20-bit DSP instruction, and

a 40-bit DSP instruction,

the set of instructions to accelerate calculations within the digital signal processor of the type where D = [(A operation one B) operation two C] where operation one and operation two are separate signal processing operations.

34. (New) The instruction set architecture (ISA) of claim 33, wherein

the twenty bit instruction uses mode bits in control registers and the forty bit instruction has a control extension to override the mode bits.

35. (New) The instruction set architecture (ISA) of claim 33, wherein

the digital signal processing operations are of the set of operations of multiplication, addition, extremum, and no operation.

36. (New) The instruction set architecture (ISA) of claim 35, wherein,

the twenty bit instruction uses mode bits in control registers and the forty bit instruction has a control extension to override the mode bits.

37. (New) The instruction set architecture (ISA) of claim 36 for execution of operations within a digital signal processor, wherein,

the control registers are mode registers.